AMENDMENTS TO THE CLAIMS

1-50. (Canceled)

51. (Currently amended) An antenna system, comprising:

a first multi-layer ~~structure~~ Printed Circuit Board (PCB), having multiple antenna elements disposed thereon;

at least a second multi-layer ~~structure~~ PCB, which is mounted below the first multi-layer ~~structure~~ PCB, and which comprises electronic components for processing Radio Frequency (RF) signals received by the antenna elements; and

multiple RF transitions, which are mounted between the first and second multi-layer ~~structures~~ PCBs and are operative to transfer the RF signals from the first multi-layer ~~structure~~ PCB for processing by the electronic components in the second multi-layer ~~structure~~ PCB.

52. (Canceled)

53. (Currently amended) The system according to claim 51, wherein the antenna elements are tilted with respect to a plane of the first multi-layer ~~structure~~ PCB.

54. (Previously presented) The system according to claim 51, wherein the RF transitions comprise coaxial transitions.

55. (Currently amended) The system according to claim 51, wherein the antenna elements comprise microstrip elements that are disposed in respective recesses in a top surface of the first multi-layer ~~structure~~ PCB.

56. (Currently amended) The system according to claim 51, wherein the electronic components comprise one or more phase shifters, one or more amplifiers and one or more combiners, which are respectively arranged to apply phase shifting, amplification and combining to the RF signals.

57. (Currently amended) The system according to claim 56, wherein the electronic components are arranged to electronically steer a beam pattern formed by the antenna elements in an elevation plane by applying the phase shifting, amplification and combining, and comprising a mechanical rotation subsystem, which is arranged to rotate the first and second multi-layer ~~structures~~ PCBs in an ~~azimouth~~ azimuth plane.

58. (New) The system according to claim 51, wherein the second multi-layer PCB has a top surface facing the first multi-layer PCB, and wherein at least one of the electronic components is disposed on the top surface of the second multi-layer PCB.